Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1-8. (Cancelled)

9. (Withdrawn) A processor comprising:

a plurality of microengines, each of the microengines comprising:

a control store, the control store storing a microprogarm loadable by a core processor;

controller logic including an instruction decoder and program counter units maintained in hardware;

context event switching logic, the context event switching logic receiving messages and arbitrating for threads;

an execution box data path including an arithmetic logic unit (ALU), general purpose registers and multiplexors providing input to the ALU;

a write transfer register stack; and

a read transfer register stack.

10. (Withdrawn) The processor of claim 9 in which the plurality of general purpose registers comprises:

a first bank of general purpose registers; and

a second bank of general purpose registers.

11. (Withdrawn) The processor of claim 10 in which the first bank general purpose registers and the second bank general purpose registers are windowed.

12. (Withdrawn) The processor of claim 9 in which registers contained in the write transfer register stack and registers contained in the read transfer register track are windowed.

13. (Withdrawn) The processor of claim 9 in which the write transfer register stack stores write data to a resource.

14. (Withdrawn) The processor of claim 9 in which the read transfer register stack stores return data from a shared resource.

15. (Withdrawn) The processor of claim 9 in which the execution box data path maintains a five-stage micro-pipeline.

16. (Withdrawn) The processor of claim 15 in which the five-stage micro-pipeline comprises:

lookup of micro-instruction words;

formation of general purpose register file addresses;

read of operands from the general purpose registers;

ALU shift or compare operations; and

write-back of results to the general purpose registers.

17. (Currently amended) A hardware-based multithreaded processor comprising:

a plurality of microengines, each of the microengines comprising a context event arbiter, a controller, a control store, local read and write transfer registers, local general purpose registers and an arithmetic logic unit (ALU), each of the microengines supporting instructions that perform an ALU operation on one or two operands, deposit a result in a destination register and update ALU condition codes according to the result; and

a local register instruction that loads one or more specified bytes within a local destination register with a shifted value of another operand.

18. (Previously presented) The processor of claim 17 wherein the destination register is an absolute transfer register.

19. (Previously presented) The processor of claim 17 wherein the destination register is a context-relative transfer register.

20. (Previously presented) The processor of claim 17 wherein the destination register is a general purpose register.

21. (Previously presented) The processor of claim 17 wherein the local register instruction comprises the destination register.

22. (Currently amended) The processor of claim 17 wherein the local register instruction comprises a field representing a mask that specifies which byte or bytes of the destination register are affected.

23. (Previously presented) The processor of claim 22 where in the mask is 4-bits.

24. (Previously presented) The processor of claim 22 wherein the mask comprises a set bit indicating a corresponding byte in the local register to be loaded.

25. (Previously presented) The processor of claim 17 wherein the local register instruction comprises a context relative source register.

26. (Currently amended) Apparatus comprising:

in a hardware-based multithreaded processor comprising a plurality of microengines, each of the microengines comprising a context event arbiter, a controller, a control store, local

read and write transfer registers, local general purpose registers and an arithmetic logic unit (ALU), each of the plurality of microengines including a command that causes the ALU to load one or more specified bytes within a destination register of a selected microengine with a shifted value of another one or more bytes of a source register.

27. (Currently amended) The apparatus of claim 26 wherein the command comprises a field representing a mask that specifies which byte or bytes of the destination register are affected.

28. (Previously presented) The apparatus of claim 27 where in the mask is 4-bits.

29. (Previously presented) The apparatus of claim 27 wherein the mask comprises a set bit indicating a corresponding byte in the source register to be loaded.